

101
Mask Design System

FIGURE 1

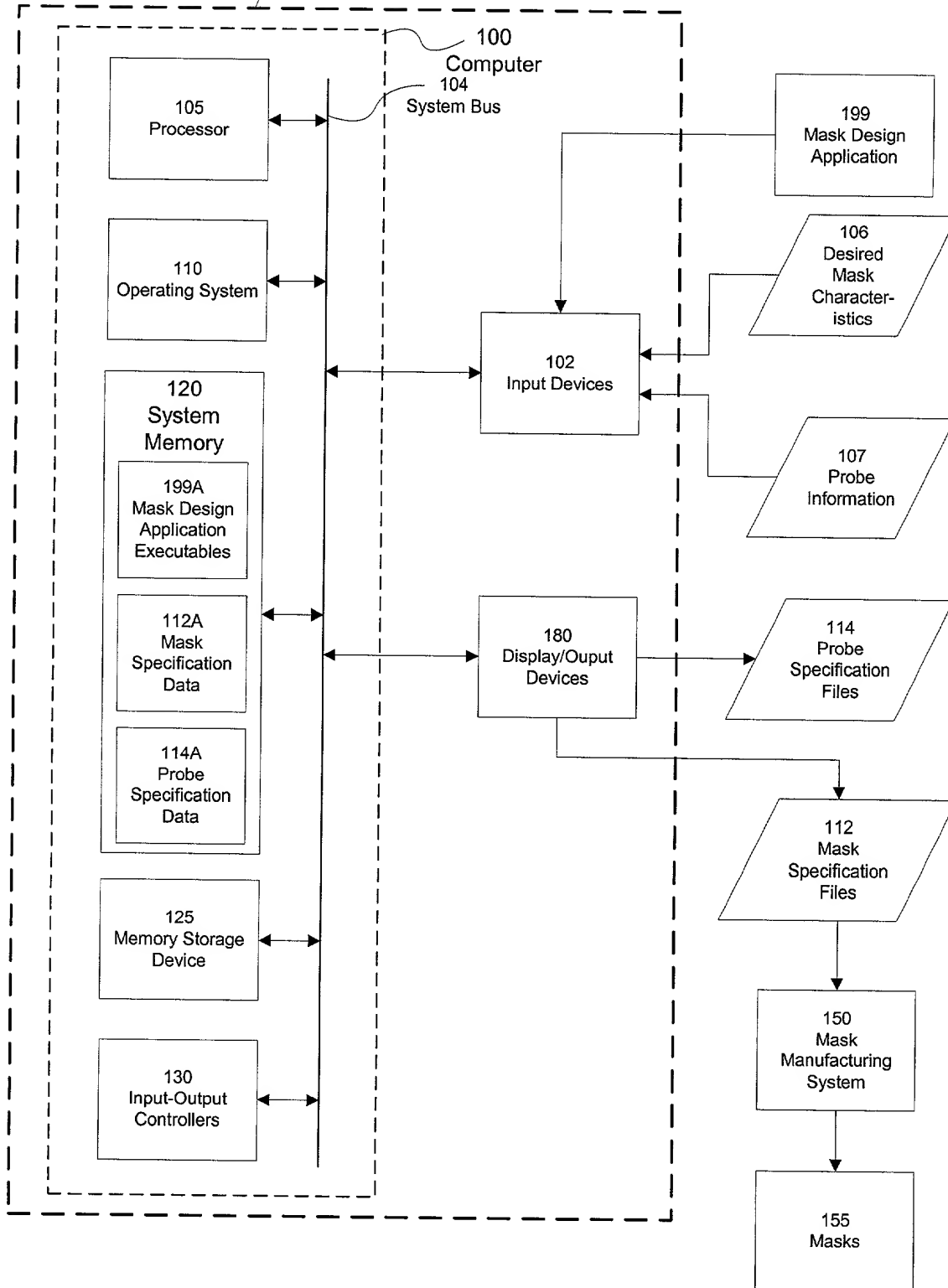
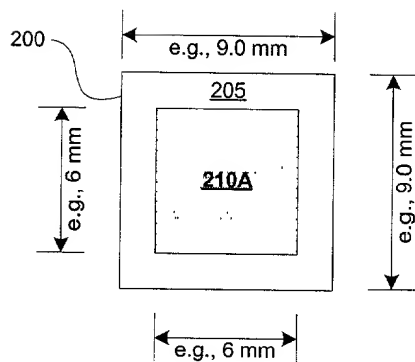


FIGURE 2A



**FIGURE 2B
(PRIOR ART)**

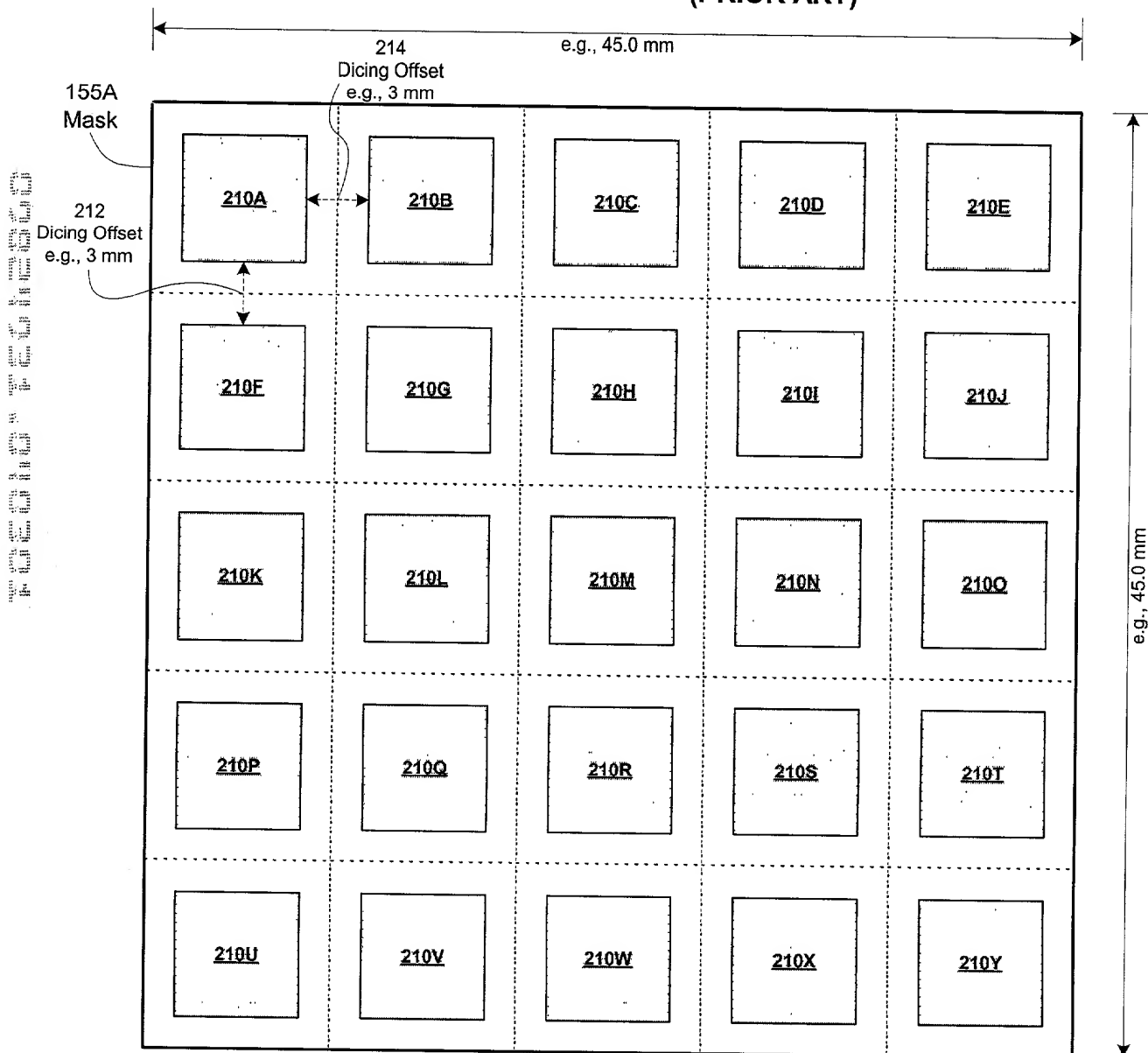
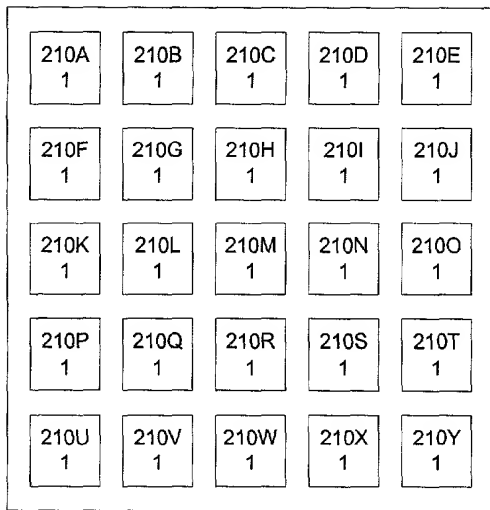


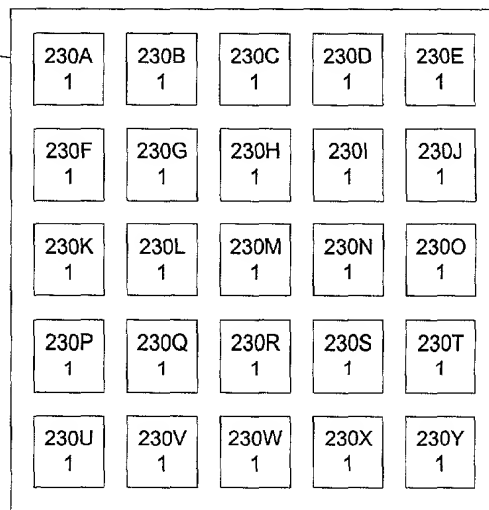
FIGURE 2C



155A-1
Mask

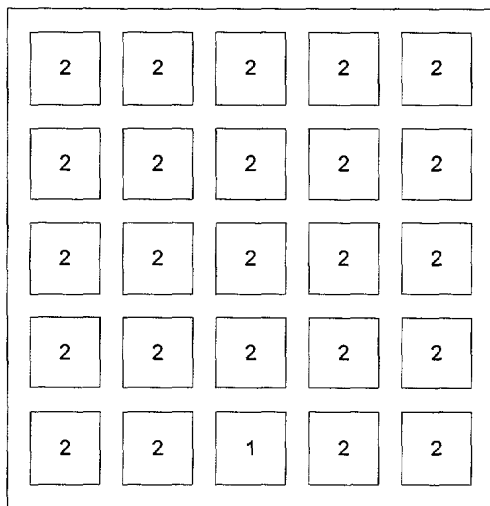
240
Wafer

FIGURE 2D



212
Dicing Offset
e.g., 3 mm

FIGURE 2G



155A-2
Mask

240
Wafer

FIGURE 2H

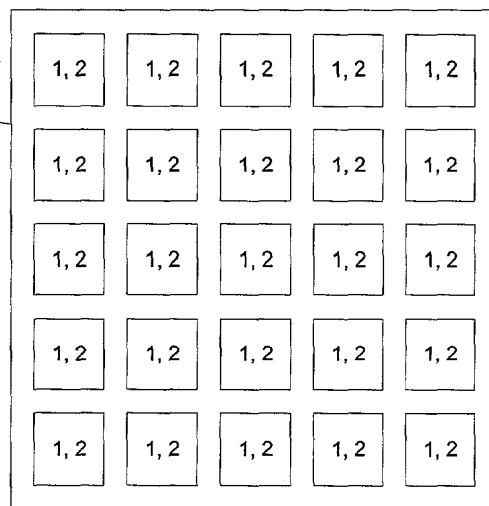
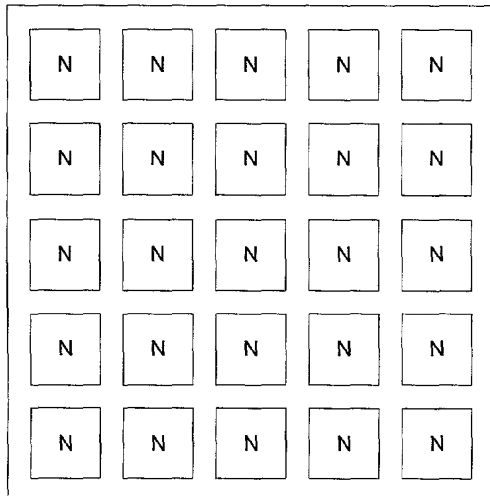


FIGURE 2E



155A-N
Mask

240
Wafer

FIGURE 2F (PRIOR ART)

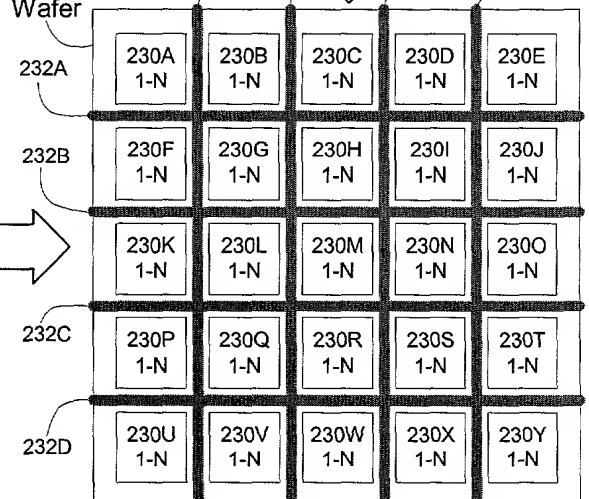
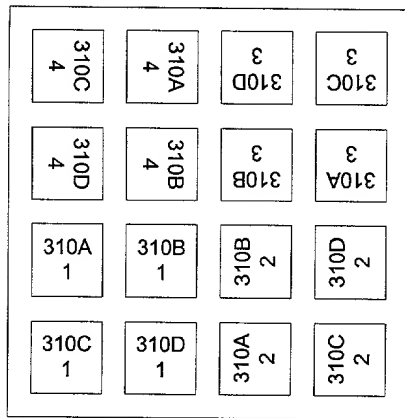


FIG. 2C is a schematic diagram of a mask 155A-1. The mask 155A-1 is a 5x5 grid of 25 cells. Each cell contains a label (210A-210Y) and the number 1. The mask 155A-1 is used to create a wafer 240. The wafer 240 is a 5x5 grid of 25 cells. Each cell contains a label (230A-230Y) and the number 1. The wafer 240 is created by dicing the mask 155A-1. The dicing offset is e.g., 3 mm. FIG. 2D is a schematic diagram of a wafer 240. The wafer 240 is a 5x5 grid of 25 cells. Each cell contains a label (230A-230Y) and the number 1. The wafer 240 is created by dicing the mask 155A-1. The dicing offset is e.g., 3 mm. FIG. 2E is a schematic diagram of a mask 155A-N. The mask 155A-N is a 5x5 grid of 25 cells. Each cell contains the letter N. The mask 155A-N is used to create a wafer 240. The wafer 240 is a 5x5 grid of 25 cells. Each cell contains a label (230A-230Y) and '1-N'. The wafer 240 is created by dicing the mask 155A-N. The dicing offset is e.g., 3 mm. FIG. 2F (PRIOR ART) is a schematic diagram of a wafer 240. The wafer 240 is a 5x5 grid of 25 cells. Each cell contains a label (230A-230Y) and '1-N'. The wafer 240 is created by dicing the mask 155A-N. The dicing offset is e.g., 3 mm. The wafer 240 is divided into four horizontal sections by thick lines, labeled 232A, 232B, 232C, and 232D. The top row is labeled 234A, 234B, 234C, and 234D.

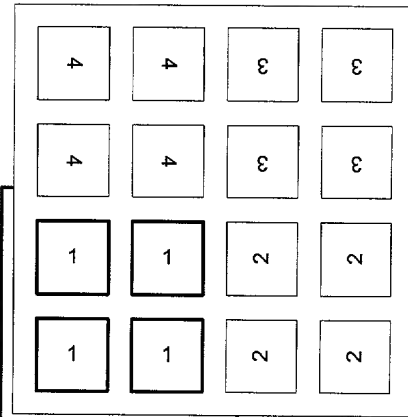
FIGURE 3A



155B
Mask

340
Wafer

FIGURE 3B



340
Wafer

FIGURE 3C

340
Wafer

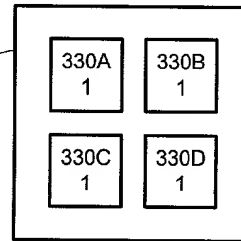


FIGURE 3C

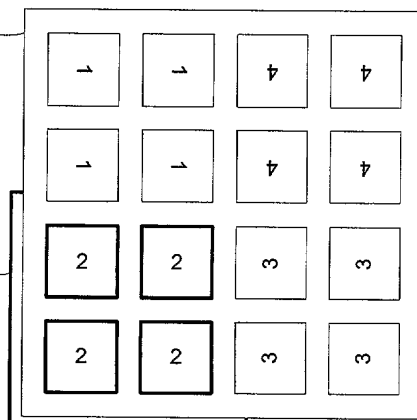
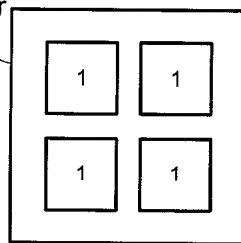
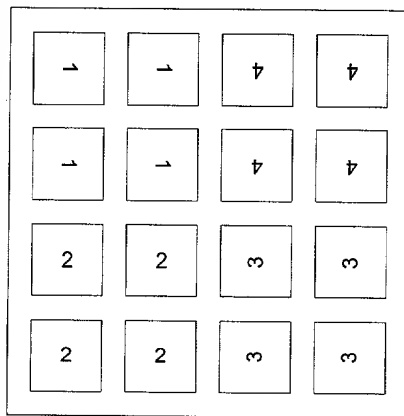
155B
Mask

340
Wafer

FIGURE 3D

155B
Mask

340
Wafer



312
Dicing Offset
e.g., 3 mm

FIGURE 3E

340
Wafer

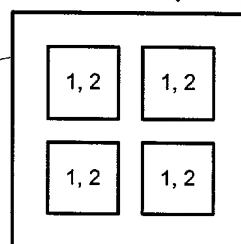


FIGURE 3F

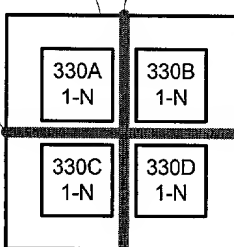


FIGURE 4A

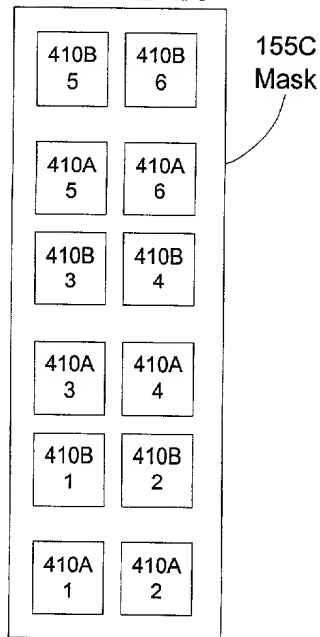


FIGURE 4B

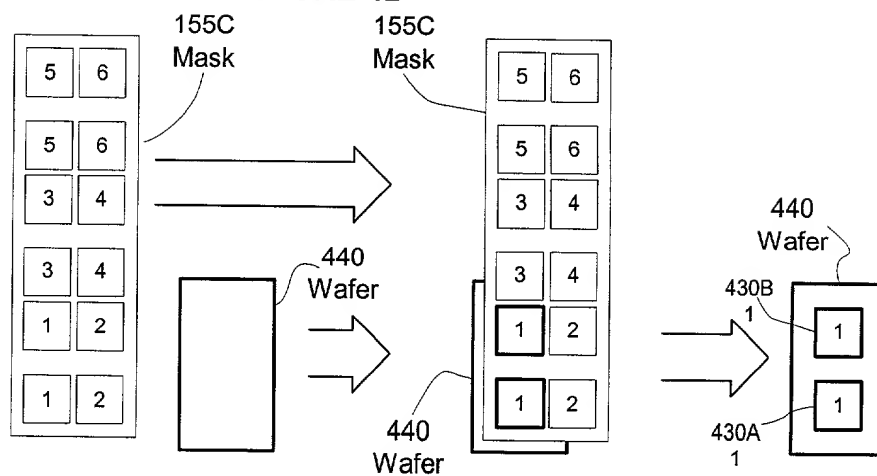


FIGURE 4C

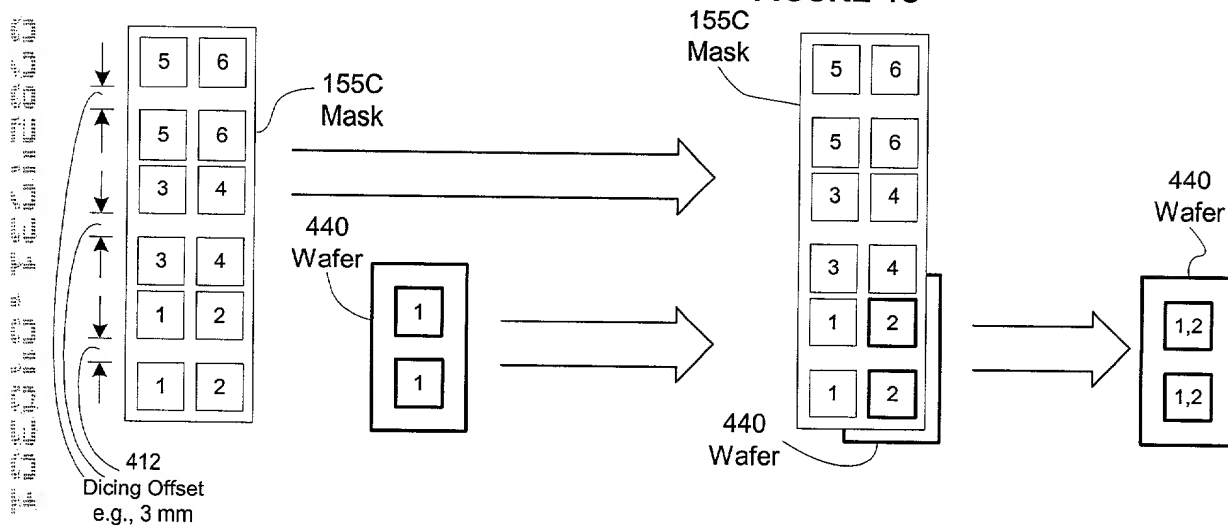


FIGURE 4D

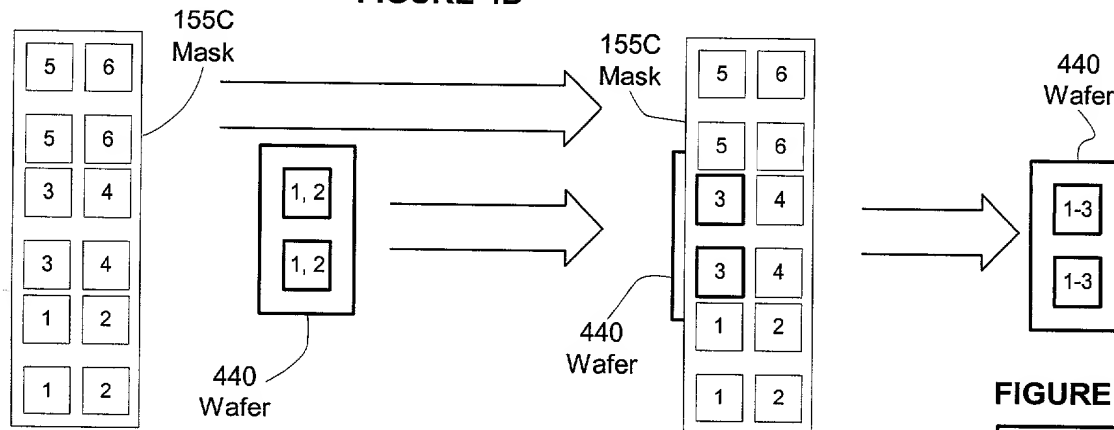


FIGURE 4E

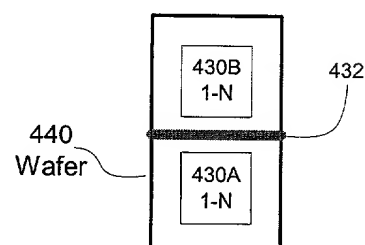


Diagram of a 510A component with dimensions:

- Top width: e.g., 4.5 mm
- Bottom width: e.g., 4.0 mm
- Left height: e.g., 4.0 mm
- Right height: e.g., 4.5 mm

FIGURE 5B

510A Interleaved Reticle Area

e.g., 9.0 mm

510A 1

510A 2

510A 4

510A 3

e.g., 9.0 mm

512 Reticle Boundaries (e.g., => 0 mm)

FIGURE 6A

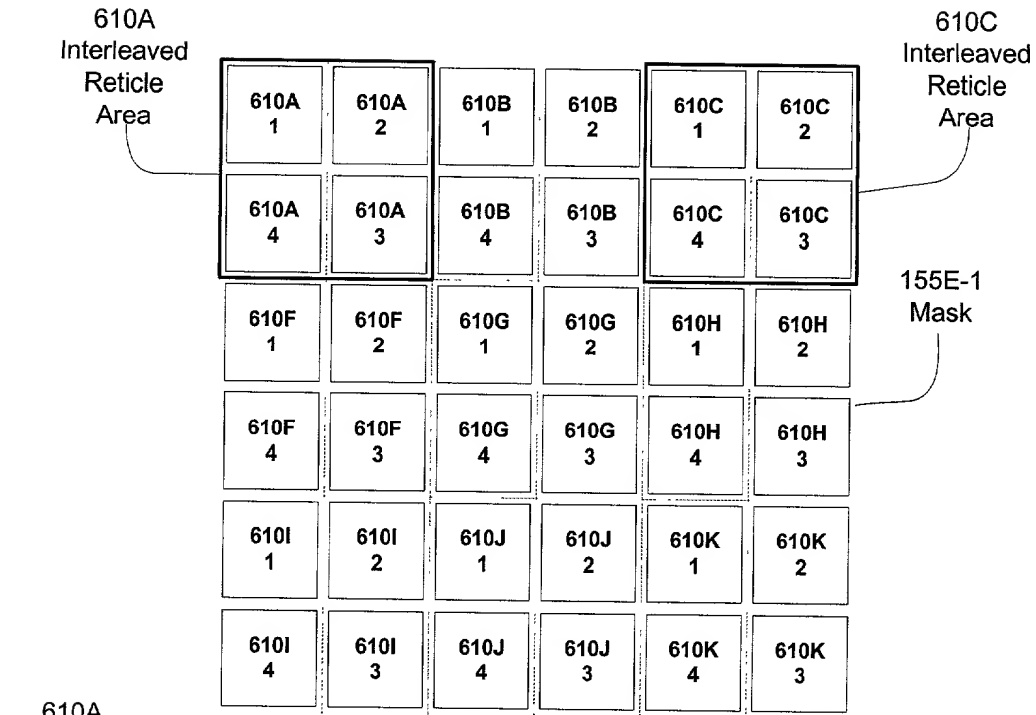


FIGURE 6B

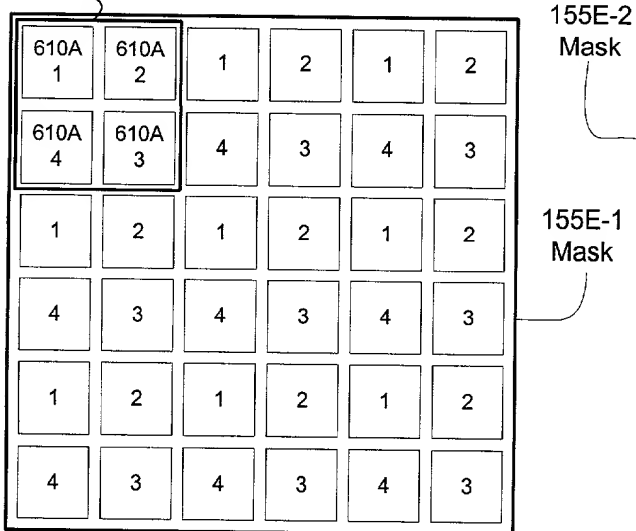


FIGURE 6C

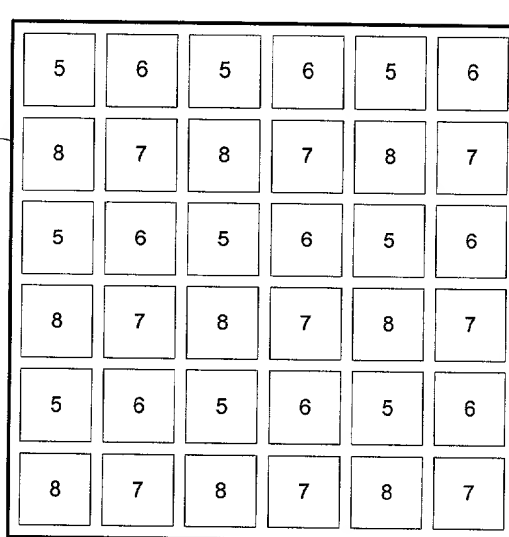


FIGURE 6D - STEP 1

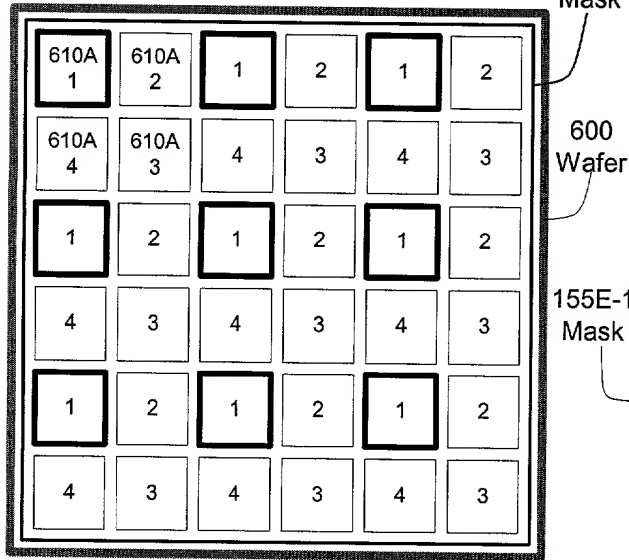


FIGURE 6E - STEP 2

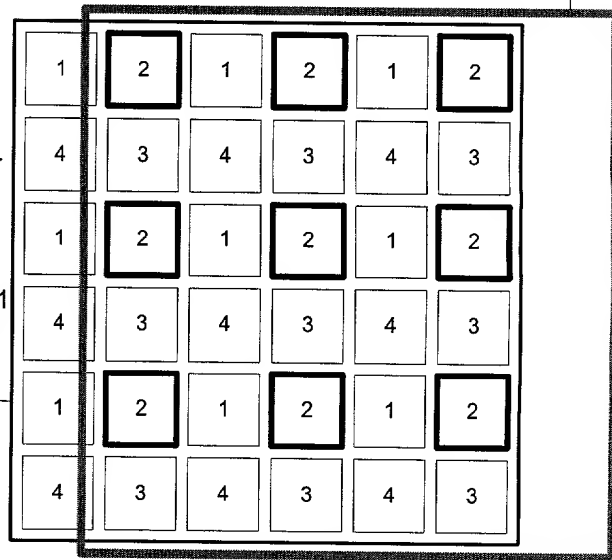


FIGURE 6F - STEP 3

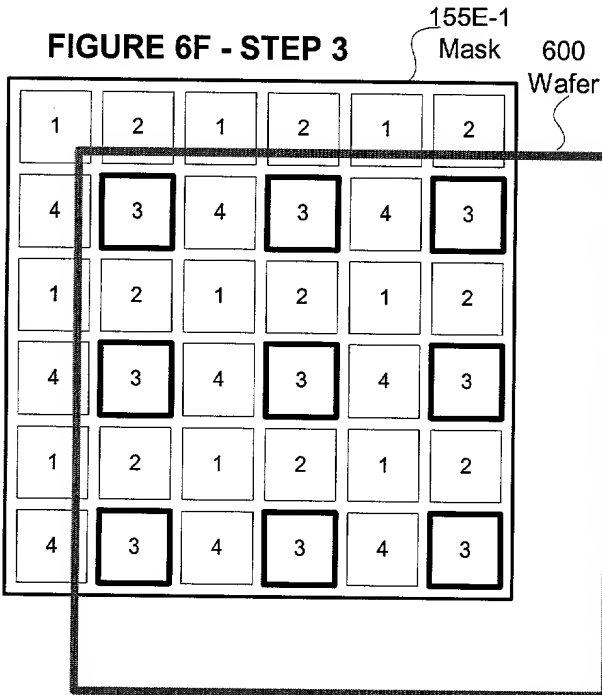


FIGURE 6G - STEP 4

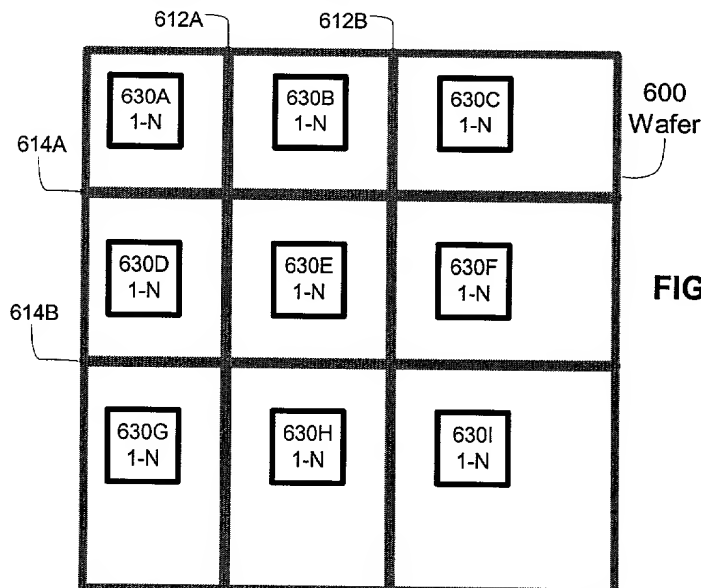
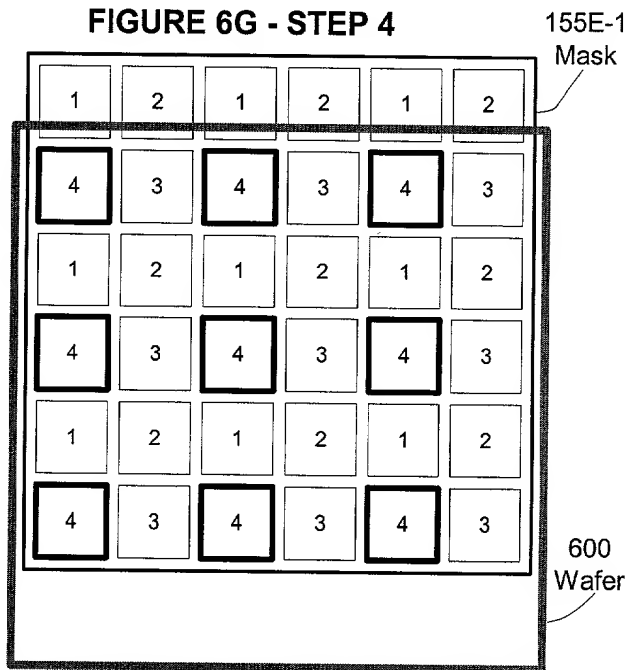
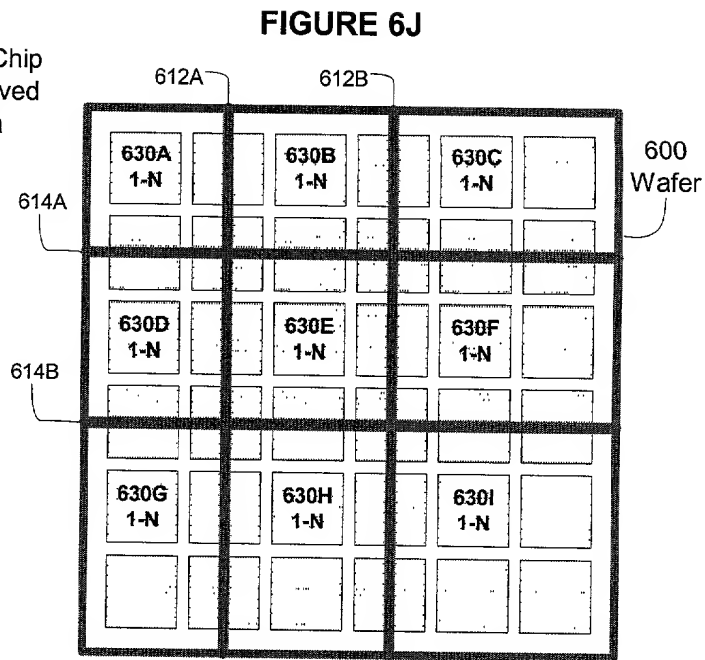
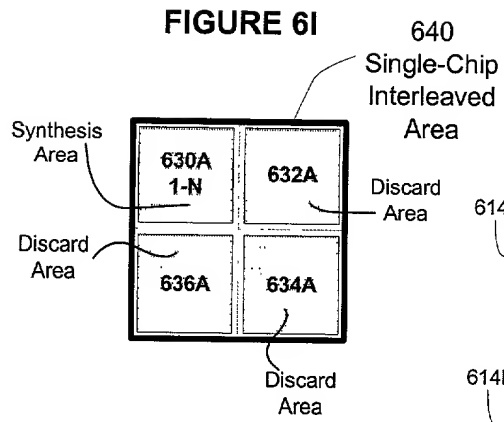


FIGURE 6H



645A Interleaved Reticle Area

FIGURE 6K

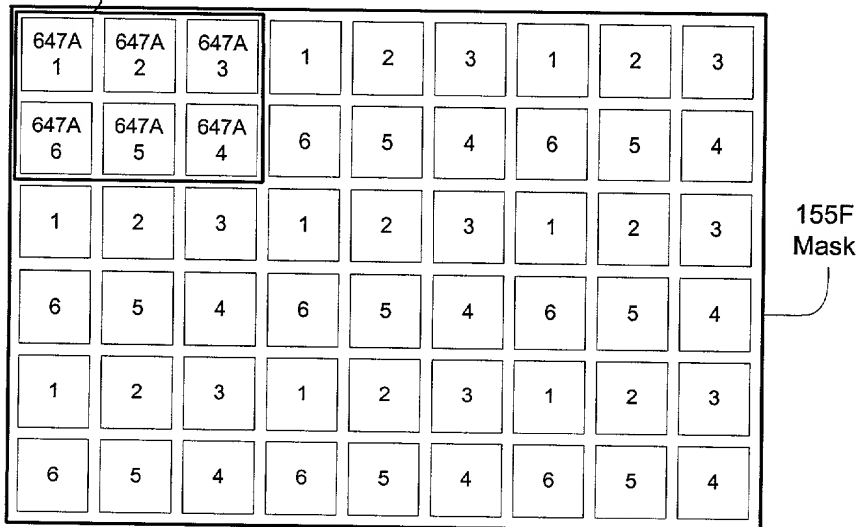


FIGURE 6L

660 Single-Chip Interleaved Area

Synthesis Area

Discard Area

Discard Area

650A 1-N

652A

654A

659A

658A

656A

Discard Area

Discard Area

Discard Area

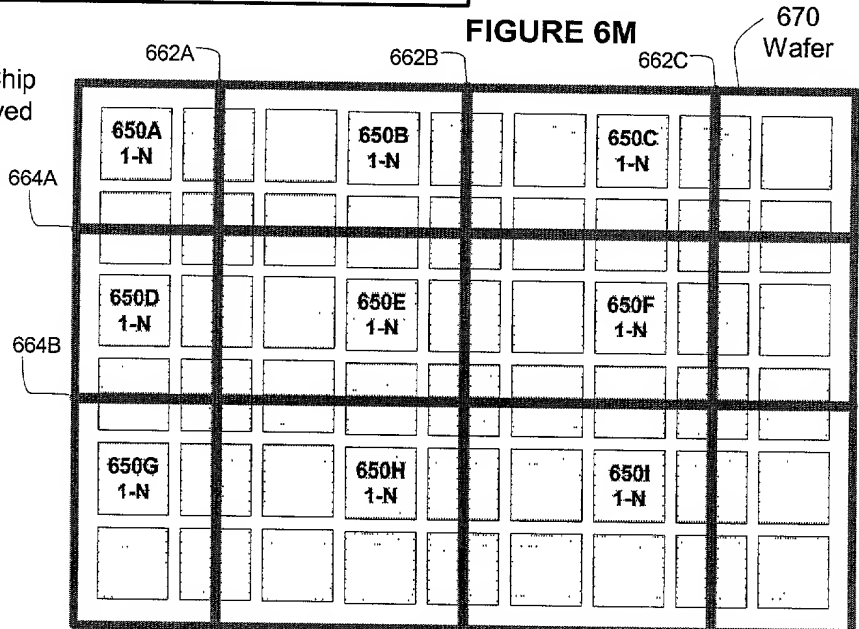


FIGURE 7

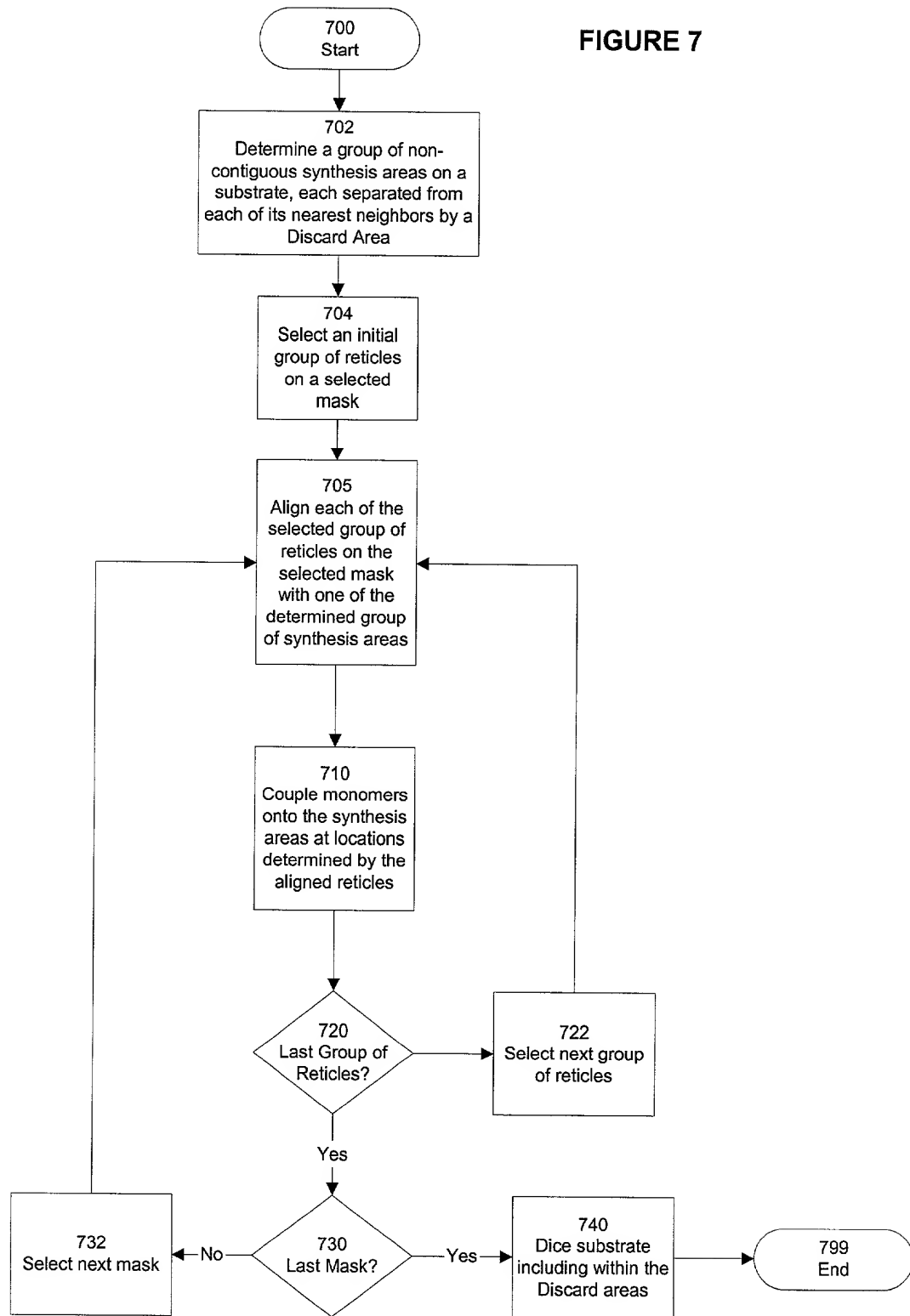


FIGURE 8

